wherein the first isolation technique and the second isolation technique are different and implemented sequentially.

5. (Amended) A system for allowing different types of isolation techniques during fabrication of a semiconductor device, comprising:

a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing, wherein the first isolation technique and the second isolation technique are different and implemented sequentially;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

9. (Amended) A semiconductor device comprising:

a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing, wherein the STI isolation technique and the LOCOS isolation technique are implemented sequentially;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.